or Abrahamson et al. (5022049). Claims 22 and 23 were rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. Claims 5 and 12 were objected to as being based upon a rejected base claim but would be allowable if rewritten in independent form.

The Examiner is requested to reconsider the rejection claims in light of the reasoning presented below. A separate sheet showing the status of all claims, in accordance with C.F.R. 121 is enclosed.

In the claim by claim analysis below it will be shown that the present application claims features not otherwise disclosed or suggested by the prior art.

<div align="center">

101 rejections
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Claims 22 and 23 were rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter.

Claim 22 of the present application specifically states:

"A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes…" [Emphasis added.]

Thus, as the Examiner points out in paragraph 3 of the subject office action, "…computer programs embodied on a computer readable medium…" are statutorily patentable. Moreover, the Applicants respectfully direct the Examiner's attention to the MPEP Sec. 2106.01 where it is stated that "When a computer program is recited in conjunction with a physical structure, such as a computer memory, USPTO personnel should treat the

claim as a product claim". The Examiner is also directed to In re Lowry, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994)(discussing patentable weight of data structure limitations in the context of a statutory claim to a data structure stored on a computer readable medium that increases computer efficiency) and Warmerdam, 33 F.3d at 1360-61, 31 USPQ2d at 1759 (claim to computer having a specific data structure stored in memory held statutory product-by-process claim), as well as In re Beauregard and U.S. Patent 5710578, (claim 10).

Therefore, the Applicants respectfully assert that claims 22 and 23 are patentable and should be allowed.

102(b) rejections

Claims 1-4, 9-11, 22, and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Adkisson et al (US 5257282).

Claim 1 of the present application recites the features of a receiver logic combiner adapted to generate a plurality of *relatively prime composite PN codes*, wherein *each* of the plurality of composite PN codes *are separated by a predetermined PN phase.*

As pointed out above and repeated here, Claim 1 of the present application also recites the feature of the *composite* PN codes are *separated by a predetermined PN phase.*

On the other hand, Adkisson, et al. is using n number of parallel Linear Feedback Shift Registers (LFSRs) (PN generators) merely to increase the speed of PN code generation

by n. In other words, Adkisson is only concerned about how fast the PN codes are generated and makes no suggestion or disclosure about generating prime PN codes separated by a predetermined PN phase.

Adkisson's failure to disclose or suggest generating PN codes separated by a predetermined PN phase is readily revealed by a close examination of Adkisson. First, in order for Adkisson's scheme to work, each of Adkisson's n LFSRs has to be staggered in phase by one nth of a generator's (LFSR's) sequence length (Adkisson fails to disclose this detail). For example, if 4 PN generators are used, as shown in Adkisson's Figure 1, the first generator would have to be initialized at the first chip of the PN LFSR's sequence, the second generator would have to be initialized at 1/4th of the LFSR's sequence, the third generator would have to be initialized at 1/2 of the PN LFSR's sequence, and the fourth PN code generator would have to be initialized at 3/4ths of the PN LFSR's sequence. Then, with the first four clock cycles, the multiplexer gets one chip from each generator, the first four chips in the multiplexed PN component code sequence. On the fifth clock, the generators get another (their second) clock cycle from the divided-by-four clock, and each of the PN code generators progresses by one chip, and the multiplexer picks up the next four chips with the given clock cycle and the subsequent 3 clock cycles. The issue here is that Adkisson is only staggering his generators by one nth of a generator's sequence length so that n generators can feed one multiplexer that runs at n times the speed of the n generators. This is <u>clearly not the same</u> as Adkisson achieving predetermined composite-code phases from

his component-code generators as suggested by the Examiner and as claimed herein.

It will be appreciated that the present application delays the output of one PN component code by 0, 1, 2, 3, or n chips. When this n-delayed component code is combinatorially combined with other relatively prime component codes, the composite code is deterministically shifted as a function of the n-number of chip delays. This means that the phase difference is deterministic between the composite PN code with n=0 delay and the otherwise same composite PN code with n not-equal-to-zero delay. The deterministic composite code phase shift is millions or billions of chips, but the phase shift is deterministic to the chip. Thus, the deterministic composite code phase shift is not one PN minor epoch, it is "a phase offset in the composite code equal to at least one combination epoch of the [component] codes not slipped. The composite code slip is a number (many) times the lengths of the component codes not experiencing the one or more chip delay relative to the other component codes.' It will be appreciated that with the delay of one component code by n chips, the composite PN code sequence is advanced in phase by millions or billions of chips, the exact number of which is perfectly known. This provides an immediate and effectively new code. Not only is the new code orthogonal to the unslipped version of itself, it is separated in phase from the unslipped version of itself by millions or billions of chips, far beyond any uncertainty that can be practically searched. The above features are readily claimed in pending claims 1-4, 9-11, 22, and 23. For example, claim 1 of the present application recites the features:

"...at least one receiver logic combiner adapted to generate a plurality of <u>relatively prime</u> composite PN codes, wherein each of the plurality of composite PN codes are separated by a <u>predetermined PN phase</u>."

This feature is not disclosed or suggested in Adkisson.

Likewise, claim 9 of the present application recites the features:

"...generating a first composite PN code; and generating a second composite PN code, wherein the second composite code is PN phase separated from the first composite PN code <u>by a predetermined composite code phase shift</u>."

This feature is not disclosed or suggested in Adkisson.

Claim 22 of the present application recites the feature of a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes. In addition, Claim 22 recites the features of generating a plurality of relatively prime PN component codes and combining the plurality of relatively prime PN component codes to generate a composite PN code. Claim 22 also recites the feature of generating a second plurality of relatively prime PN component codes, wherein one of the component codes is PN phase delayed, and combining the plurality of relatively prime PN component codes to generate a second composite PN code. The result is that the second composite PN code is phased delayed by a deterministic delay substantially equal to at least one combination epoch of the component codes not slipped. Nowhere does Adkisson disclose or suggest phase

delaying a component code by a predetermined phase delay, i.e., PN phase delay, to form a second composite PN code phased delayed where the phase delay is substantially equal to at least one combination epoch of component codes not slipped.

Claim 23 of the present application recites a program storage device having at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file. Nowhere does Adkisson disclose or suggest VHDL language files.

Yet, nowhere does Adkisson disclose or suggest these features of generating relatively prime composite PN codes separated by a predetermined PN phase.

Therefore, in light of the above, claims 1-4, 9-11, 22, and 23 are patentable and should be allowed.

103(a) rejections

Claims 6-8 and 13-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al in view of Kartchner et al. (US 4638494) or Abrahamson et al. (5022049).

Dependent claims 6-8, and 13-18 all recite the features of MAND, MAJ, or MOD logic combination of the relatively prime PN codes. As pointed out earlier and repeated here Adkisson fails to disclose or suggest the parent claim features of *predetermined phase separation between relatively prime composite codes* from which these claims depend. In addition, neither does Kartchner et al., or Abrahamsom et al., disclose or suggest MAND, MAJ, or MOD logic combination of the

relatively prime PN codes where one of the combination codes has been PN phased delayed by a predetermined amount.

Therefore claims 6-8 and 13-18 are patentable and should be allowed.

Allowable Claims

Claims 5 and 12 were objected to as being based upon a rejected base claim but would be allowable if rewritten in independent form.

Claim 5 has been rewritten in independent form as new claim 24. Claim 9 has been amended to include the limitations of claim 12 and any intervening claims. Therefore, claim 9 and its progeny should be in a condition for allowance.

The Applicants respectfully assert that all of the pending claims are now in a condition for allowance.

Filed concurrently within pair is the fee for one independent claim over 3 independent claims. Should any unresolved issue remain, the Examiner is invited to call Applicant's Attorney at the telephone number indicated below.

Respectfully submitted,

/Kevin P. Correll/   June 7, 2008

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Kevin P. Correll (Reg. No. 46,641)   Date

K. P. Correll & Associates, LLP
270 Bellevue Ave, #326
Newport, RI 02840
V: (401) 295-7377
F: (401) 295-9054